



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:

Mark I. Gardner et al.

Serial No. 09/207,972

Filed: December 9, 1998

For: Ultrathin High-K Gate Dielectric
with Favorable Interface Properties
for Improved Semiconductor Device
Performance

§ Group Art Unit: 2815

§ Examiner: Warren, Matthew E.

§ Atty. Dkt. No.: 5500-36101

§ TT2823CPA

**CERTIFICATE OF MAILING
37 C.F.R. § 1.8**

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on the date indicated below:

Robert C. Kowert
Name of Registered Representative

March 12, 2003
Date

[Signature]
Signature

APPEAL BRIEF

Box AF

Commissioner for Patents
Washington D.C. 20231

Sir/Madam:

Further to the Notice of Appeal submitted herewith, Appellants present this Appeal Brief. Appellants respectfully request that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The subject application is owned by Advanced Micro Devices, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at One AMD Place, Sunnyvale, CA 94088, as evidenced by the assignments recorded at Reel/Frame 009664/0015 and Reel/Frame 009664/0037.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-22 were presented in the original application. Subsequently, claims 1-15 were cancelled and claims 23-33 were added. Claims 16-33 are pending. Claims 24-29, 32 and 33 are allowed. Claim 22 is objected to. Claims 16-21, 23, 30 and 31 stand finally rejected under 35 U.S.C. § 103(a) and are the subject of this appeal. A clean copy of claims 16-21, 23, 30 and 31, as on appeal, is included in Appendix A herewith.

IV. STATUS OF AMENDMEMNTS

No amendments to the claims have been filed subsequent to the final rejection. Appendix A herewith reflects the current state of the claims on appeal.

V. SUMMARY OF THE INVENTION

Thin gate dielectrics for integrated devices are desirable to accommodate scaling and improve device performance. *See* specification p. 1, line 12 - p. 2, line 22. Unfortunately, thin gate oxides may be subject to problems such as electron tunneling, charge accumulation and defects. *See* specification p. 2, line 24 - p. 3, line 8. Thicker

gate dielectrics having a higher dielectric constant K than silicon dioxide may be used to address the problems associated with thin gate oxides. However, high-K dielectrics may not interface well with the semiconductor substrate. *See* specification p. 3, line 10 - p. 4, line 13.

In an embodiment of the present invention, a semiconductor device may have a graded-K gate dielectric. A gate conductor 18 may be arranged above the graded-K gate dielectric. *See, e.g.*, Fig. 5. In one embodiment, the graded-K gate dielectric may include a low-trap-density nitrogen-containing oxide 12 arranged upon an upper surface of a semiconductor substrate 10 and a high-K dielectric 16 having a dielectric constant greater than about 5 arranged upon the nitrogen-containing oxide 12. *See, e.g.*, specification p. 14, line 20 - p. 16, line 30; Figs. 5 & 6. The low-trap-density nitrogen-containing oxide portion of the graded-K gate dielectric may be fabricated to have favorable interface properties with the semiconductor substrate. *See, e.g.*, specification p. 11, line 4 - p. 14, line 18; Figs. 1-4. The nitrogen content of the oxide may increase its K value and may make it more resistant to dopant impurity diffusion.

VI. ISSUES

1. Whether claims 16-19, 21, 23, 30 and 31 are patentable under 35 U.S.C. § 103(a) over Kizilyalli et al. (U.S. Pat. No. 6,320,238) (hereinafter “Kizilyalli”) in view of Wu (U.S. Pat. No. 5,880,508).

2. Whether claim 20 is patentable under 35 U.S.C. § 103(a) over Kizilyalli in view of Wu as applied to claim 16, and further in view of Chou (U.S. Pat. No. 5,994,734).

VII. GROUPING OF CLAIMS

Claims 16-21, 23, 30 and 31 stand or fall together for purposes of this appeal only.

VIII. ARGUMENT

Claims 16-19, 21, 23, 30 and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,320,238 to Kizilyalli et al. (hereinafter “Kizilyalli”) in view of U.S. Patent No. 5,880,508 to Wu (hereinafter “Wu”). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kizilyalli in view of Wu as applied to claim 16, and further in view of U.S. Patent No. 5,994,734 to Chou (hereinafter “Chou”). Appellants respectfully traverse these rejections in light of the following remarks.

The Kizilyalli patent does not qualify as prior art. Kizilyalli was filed on June 25, 1999 and is a continuation-in-part of application no. 08/995,435, filed on December 22, 1997. Since the filing date of the Kizilyalli patent is after the filing date of the present application, Kizilyalli may only be applied as prior art if it is entitled to the filing date of its parent application no. 08/995,435. The filing date of the Kizilyalli patent’s parent application no. 08/995,435 can only be used as the prior art date if the parent supports the claims of the child continuation-in-part reference (the claims of the Kizilyalli patent). *See* M.P.E.P. § 2136.03(IV). However, none of the claims of the Kizilyalli patent are supported by its parent application. Both of the independent claims of the Kizilyalli patent include limitations not supported in its parent application no. 08/995,435. Kizilyalli’s claim 1 includes the limitation of “said dielectric material layer having an equivalent electrical thickness of 2.2 nm or less.” A copy of Kizilyalli’s parent application no. 08/995,435 as originally filed is included herewith as Appendix B. The above-quoted limitation from claim 1 of the Kizilyalli patent is neither described nor enabled in application no. 08/995,435. The other independent claim (claim 11) of the Kizilyalli patent includes the limitation of “an electrode disposed directly on said at least one layer of high-k dielectric material.” (emphasis added). This limitation is neither described nor enabled in application no. 08/995,435. Since the claims of the Kizilyalli patent are not supported by its parent application, the Kizilyalli patent is not entitled to the filing date of its parent application. Therefore, the Kizilyalli patent may not be applied as prior art against Appellants’ application.

Additionally, only the material that is common to both the Kizilyalli patent and its parent is eligible as potential prior art. *In re Wertheim*, 209 USPQ 554 (CCPA 1981). The Examiner relies on the structure illustrated in Fig. 1 of the Kizilyalli patent to reject Appellants' claims. However, Fig. 1 of the Kizilyalli patent illustrates an embodiment in which the gate electrode 104 is disposed directly on the high-k dielectric material 103 and in which the equivalent electrical thickness of the dielectric material layer is 2.2 nm or less. This embodiment is not described nor enabled in the Kizilyalli patent's parent application. Therefore, the material in the Kizilyalli patent used to reject Appellants' claims is not prior art to Appellants' application.

IX. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 16-21, 23, 30 and 31 was erroneous, and reversal of the Examiner's decision is respectfully requested.

This Appeal Brief is submitted in triplicate along with the following items:

- ☒ Return Receipt Postcard
- ☒ Copy of U.S. Patent Application 08/995,435 as originally filed
- ☒ Notice of Appeal
- ☒ Petition for a One Month Extension of Time
- ☒ Deposit Account Fee Authorization form for the \$110.00 extension of time fee, the \$320.00 notice of appeal fee and the \$320.00 appeal brief fee.

Respectfully submitted,



Robert C. Kowert

Reg. No. 39,255

Attorney for Appellants

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Date: March 12, 2003

X. APPENDIX A

The claims on appeal are as follows.

16. A semiconductor device, comprising:

a low-trap-density nitrogen-containing oxide arranged upon an upper surface of a semiconductor substrate;

a high-K dielectric having a dielectric constant greater than about 5 arranged upon the nitrogen-containing oxide; and

a gate conductor arranged above the high-K dielectric.

17. The device as recited in claim 16, wherein said high-K dielectric comprises silicon nitride.

18. The device as recited in claim 16, wherein said high-K dielectric comprises a material having a dielectric constant greater than about 20.

19. The device as recited in claim 17, further comprising a dielectric having a dielectric constant greater than about 20 arranged upon the silicon nitride.

20. The device as recited in claim 16, further comprising:

an additional gate conductor interposed between the nitrogen-containing oxide and the semiconductor substrate; and

a gate dielectric arranged interposed between the additional gate conductor and the semiconductor substrate.

21. The device as recited in claim 16, wherein said nitrogen-containing oxide has a thickness of less than about 10 angstroms.

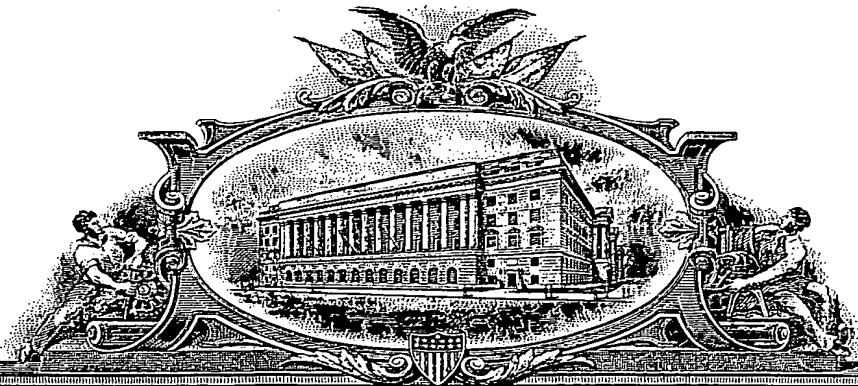
23. The device as recited in claim 16, wherein said high-K dielectric comprises a metal oxide having a dielectric constant greater than about 20.

30. The device as recited in claim 16, wherein said high-K dielectric has a low-trap-density.

31. The device as recited in claim 16, wherein said low-trap-density nitrogen-containing oxide and said high-K dielectric form a gate dielectric, wherein said gate dielectric has a low-trap-density.

XI. APPENDIX B

The following is a copy of U.S. Patent Application No. 08/995,435.



THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

March 05, 2003

**THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM
THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK
OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT
APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A
FILING DATE UNDER 35 USC 111.**

APPLICATION NUMBER: 08/995,435

FILING DATE: December 22, 1997

**By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS**



W. Montgomery
W. MONTGOMERY
Certifying Officer

THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Isik C. Kizilyalli
Yi Ma
Pradip Kumar Roy

A

"Express Mail" mailing label
Number EH560630890US
Date of Deposit Dec 22 1997
I hereby certify that this application is
being deposited with the United States Postal
Service "Express Mail Post Office to
Addressee" service under 37 CFR 1.10 on the
date indicated above and is addressed to the
Commissioner of Patents and Trademarks
Washington, D. C. 20231.
Janet M. Garger
(Printed name of person mailing paper or fee)
Janet M. Garger
(Signature of person mailing paper or fee)

CASE 9-9-33

TITLE Compound, High-K, Gate And Capacitor Insulator Layer

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification
1 Formal sheet of drawing
Declaration and Power of Attorney
Preliminary Amendment

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	15 - 20 =	0	x \$22 =	\$0
Independent Claims	2 - 3 =	0	x \$82 =	\$0
Multiple Dependent Claim(s), if applicable			\$270 =	\$0
Basic Fee				\$790
TOTAL FEE:				\$790

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of \$790, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Please address all correspondence to **Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P. O. Box 636, Murray Hill, New Jersey 07974-0636**. However, telephone calls should be made to me at 610-712-5118.

Respectfully,

Scott W. McLellan
Scott W. McLellan
Reg. No. 30776
Attorney for Applicant(s)

Date: December 22, 1997

Lucent Technologies Inc.
600 Mountain Avenue
P. O. Box 636
Murray Hill, New Jersey 07974-0636

12/22/97

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Compound, High-K, Gate and Capacitor Insulator Layer

Background of the Invention

Cross-Reference to Related Application

- This application claims priority of Provisional Application Serial No.
5 60/033839 which was filed on December 23, 1996.

This application is related to a co-pending patent application titled
"Method of Making a Compound, High-K, Gate and Capacitor Insulator Layer", by
Kizilyalli et al., serial number 08/995,589, filed simultaneously with, and assigned
to the same assignee, as this application.

10 Field of the Invention

This invention relates to integrated circuits in general and, more
particularly, to gate/capacitor dielectrics having a high dielectric constant (high K).

Description of the Prior Art

- As feature sizes on integrated circuits gets smaller, the amount of
15 capacitance for a given circuit element decreases, such as with a memory storage
capacitor, and operating voltages are decreased.

- For a transistor to operate reliably at lower voltages, the threshold
voltage of the transistor is correspondingly lowered. One approach to lower the
threshold voltage is to thin the insulating layer (usually a single layer of silicon
20 dioxide) separating the transistor gate from the transistor channel. But at very thin
insulating thicknesses (e.g., an oxide layer thickness of less than 3.5 nm), the oxide
layer suffers from pinholes and leakage may be too large. Further, if the oxide layer
is less than 2.5 nm, tunneling of electrons from the transistor channel may occur,
degrading transistor performance. Alternatively, the gate may be effectively
25 "moved" closer to the channel by incorporating a high dielectric constant (k)
material as the gate insulator between the gate and the transistor channel. However,
this approach with high-k materials (such as ferroelectric dielectrics) has not been
entirely satisfactory because of defects within the dielectric and also at the
silicon/dielectric interface, due for example by lattice mismatch, causing excessive
30 gate to substrate leakage.

- The reduced feature size and lower operating voltage is of special
concern with dynamic memories where capacitors are used to store information. As
more memory cells are added to a given memory array and feature sizes are
decreased so that the extra cells can be added within a reasonable chip size, the size
35 of the storage capacitors are correspondingly decreased. With lower capacitance of
the storage capacitors and reduced voltage on the capacitors, the memory may
become more error prone. To compensate for the reduction in capacitor size and still
maintain capacitance, two approaches can be used singly or in combination:

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dielectric thinning and increasing the dielectric constant. But the same problems with both approaches discussed above apply here as well.

- From a practical point of view, the use of high-k materials may be the most desirable choice to solve the above problems at feature sizes of 0.35 μm and below if the leakage/defects problems can be satisfactorily solved.

Therefore, there exists a need for incorporating high dielectric materials into integrated circuit designs with reduced defect and leakage problems of the heretofore approaches of device fabrication incorporating high dielectric constant materials.

10 Summary of the Invention

- This and other aspects of the invention may be obtained generally with an integrated circuit having an oxidizable layer having a surface, such as a silicon substrate or a polysilicon layer, having: a grown oxide layer on the oxidizable surface, a high-k dielectric layer on the grown oxide layer, and a deposited oxide layer on the high-k dielectric layer. Preferably, the grown oxide layer is grown from the substrate or polysilicon layer.

Brief Description of the Drawing

- The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following detailed description of the drawings, in which:

FIG. 1 is a cross section of a partially formed exemplary transistor having a gate oxide fabricated according to one embodiment of the invention; and

- FIG. 2 is a cross section of a partially fabricated exemplary polysilicon-to-polysilicon capacitor with an dielectric layer fabricated according to another embodiment of the invention.

Detailed Description

- Generally, the invention may understood by referring to FIG. 1. As discussed below in more detail and in accordance with one embodiment of the invention, an integrated circuit including a wafer 1 having an oxidizable layer 2, here a silicon substrate but may be any oxidizable layer such as a polysilicon layer, has thereon a grown oxide layer 3, the layer 3 being preferably an oxide of the substrate 2. On the layer 3 is a layer of a high dielectric constant material 4 (referred to herein as a high-k dielectric material), to be described below. Over layer 4 is a deposited oxide layer 5. Preferably, the deposited oxide layer 5 is densified.

- In more detail and describing how the wafer 1 is made, the wafer 1 includes an exemplary silicon substrate 2 which has grown thereon an oxide layer 3, here a silicon dioxide layer with the silicon ^{becoming} ~~coming~~ substantially the substrate 2. The layer 3 is preferably grown in a conventional dry oxidizing atmosphere at 0.25

to 10 torr and 650° to 900°C to form 1 to 2 nm thick oxide, the thicknesses not being critical but of sufficient thickness to avoid substantial pinhole formation and a good substrate/oxide interface. While the oxide is preferably grown in a dry atmosphere, it may be grown in a wet (steam) atmosphere.

5 The layer 3 is believed to help reduce strain between the later deposited high-k dielectric layer 4 and the underlying silicon substrate 2 and provides a good interface with the silicon to reduce undesired surface states in the silicon. Without the layer 3, it is believed that a lattice mismatch between the substrate 2 and the later deposited layer 4 creates defects at the interface between the layers, decreasing the
10 overall quality of the dielectric.

Over the grown dielectric layer 3 is deposited a layer or layers 4 of a high-k dielectric material, such as a ferroelectric dielectric material, this material having a dielectric constant greater than that of silicon dioxide. This material may be of group of materials including Ta_2O_5 , TiO_2 , SrO_3 , and perovskite materials of
15 the form $MTiO_3$, where M may be Sr, Ba, La, Pb, Ba_xSr_{1-x} , and Pb_xLa_{1-x} . It is understood that combinations of these layers may be used or interposed insulating layers, such as silicon dioxide, may be added. Exemplary thickness of the layer 4 are from 2 to 20 nm and done in a plasma enhanced, ion-beam assisted, or ozone low pressure chemical vapor deposition (LPCVD) or metalorganic chemical vapor
20 deposition (MOCVD) processes. Examples of these processes are as disclosed in "Preparation of (Ba, Sr)TiO₃ Thin Films by Chemical Vapor Deposition using Liquid Sources," by T. Kawahara et al., Japanese Journal of Applied Physics, V33, no. 10, 1994, pp. 5897 - 5902, and "Preparation of PbTiO₃ Thin Films by Plasma Enhanced Metalorganic Chemical Vapor Deposition," by E. Fujii et al., Applied
25 Physics Letters, Vol. 65, no. 3, 1994, pp. 365 - 367, included herein by reference.

After the formation of layer 4, a layer 5 of silicon dioxide is deposited. This layer is preferably 1 to 3 nm thick and preferably formed in a LPCVD reactor (not shown), preferably the same as that used to deposit layer 4. Typical source gasses for the silicon include tetraethylorthosilicate gases (TEOS) or silane.

30 The layer 5 is preferably densified by exposing the wafer 1 to a conventional densification anneal process in an oxidizing ambient atmosphere. An example of such a process step is in an LPCVD reactor operating at a pressure of 250 millitorr to 10 torr with temperatures between 650° and 900°C for approximately 5 - 20 minutes. The oxidizing atmosphere may include N_2O to add nitrogen to the
35 layer 5.

The densification step helps improves the overall quality of the layer 5, remove traps (defects) in the layers 3 - 5, and reduces the overall leakage through the layers 3 - 5.

An exemplary conductive layer 6, such as polysilicon, is shown on layer 5. This layer 6 may be a gate or one plate of a capacitor (the other plate being the substrate 2 or an upper layer not shown), the combination of layers 3 - 5 being referred to herein as a gate or capacitor insulating layer. It is understood that the densification step described above may be done after the formation of layer 6 with the attendant oxidation of the layer 6 if unprotected.

An alternative embodiment is shown in FIG. 2 for an exemplary capacitor structure. Here a wafer 10 has thereon an insulating layer 12 to separate an exemplary oxidizable and conductive layer 13, such as amorphous or polysilicon (the amorphous silicon being rendered conductive at a later step). Layers 14 - 16 correspond to layers 3 - 5 in FIG. 1 as described above. Layer 17, also preferably a conductive layer, along with layer 13 forms the plates of a capacitor while layers 14 - 16 form the capacitor insulating layer.

While silicon is described as the material type for the substrate and other layers, it is understood that other materials may be used, such as GaAs, InP, etc.

Having described the preferred embodiment of this invention, it will now be apparent to one of skill in the art that other embodiments incorporating its concept may be used. Therefore, this invention should not be limited to the disclosed embodiment, but rather should be limited only by the spirit and scope of the appended claims.

The invention claimed is:

1. ~~An integrated circuit having an oxidizable layer with a surface~~
 2 comprising:
 3 ~~a grown oxide layer on the oxidizable surface;~~
 4 ~~a high-k dielectric layer on the grown oxide layer; and~~
 5 ~~a deposited oxide layer on the high-k dielectric layer.~~
2. The integrated circuit as recited in claim 1, wherein the deposited
 oxide layer is a densified deposited oxide layer.
3. The integrated circuit as recited in claim 2, wherein the high-k
 dielectric layer is selected from the group of ^{consisting} ~~Ta₂O₅, TiO₂, and perovskite~~
 materials.
4. The integrated circuit as recited in claim 2, wherein the perovskite
 material ^{materials are} ~~is~~ of the form MTiO₃, where M is selected from the group of Sr, Ba, La, Ti,
 Pb, Ba_xSr_{1-x} and Pb_xLa_{1-x}.
5. The integrated circuit as recited in claim 2, wherein the oxide layers
 are oxides of silicon.
6. The integrated circuit as recited in claim 5, wherein oxidizable layer is
 a silicon substrate.
7. The integrated circuit as recited in claim 5, wherein oxidizable layer is
 a polysilicon layer.
8. The integrated circuit as recited in claim 5, further comprising ~~step of~~
 a conductive layer on the deposited oxide layer.
9. The integrated circuit as recited in claim 5, wherein the combination
 of layers forms a gate insulating layer.
10. The integrated circuit as recited in claim 5, wherein the combination
 of layers forms a capacitor insulating layer.
11. ~~An integrated circuit having a silicon substrate with a surface,~~
 comprising:

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densified

a grown silicon dioxide layer on the substrate surface;
a high-k dielectric layer on the grown silicon dioxide layer; and
a deposited, densified silicon dioxide layer on the high-k dielectric layer.

1 12. The integrated circuit as recited in claim 11, wherein the high-k
B 2 dielectric layer is selected from the group ^{consisting} of Ta_2O_5 , TiO_2 , and perovskite
3 materials.

1 13. The integrated circuit as recited in claim 12, wherein the perovskite
B 2 ^{materials are} material is of the form $MTiO_3$, where M is selected from the group of Sr, Ba, La, Ti,
3 Pb, Ba_xSr_{1-x} and Pb_xLa_{1-x} .

1 14. The integrated circuit as recited in claim 11, wherein the combination
2 of layers forms a gate insulating layer.

1 15. The integrated circuit as recited in claim 11, wherein the combination
2 of layers forms a capacitor insulating layer.

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Abstract of the Disclosure

A gate or capacitor insulator structure using a first grown oxide layer, a high-k dielectric material on the grown oxide layer, and a deposited oxide layer on the high-k dielectric material. The deposited oxide layer is preferably a densified deposited oxide layer. A conducting layer, such as a gate or capacitor plate, may overlay the densified oxide layer.

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IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Compound, High-K, Gate And Capacitor Insulator Layer** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

08995435-122297

Robert R. Axenfeld	(Reg. No. 37276)
Steven R. Bartholomew	(Reg. No. 34771)
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Richard J. Botos	(Reg. No. 32016)
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Michael A. Morra	(Reg. No. 28975)
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Katharyn E. Olson	(Reg. No. 37693)
Joseph J. Opalach	(Reg. No. 36229)
Eugen E. Pacher	(Reg. No. 29964)
Jack R. Penrod	(Reg. No. 31864)
Gregory C. Ranieri	(Reg. No. 29695)
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Charles L. Warren	(Reg. No. 27407)
Eli Weiss	(Reg. No. 17765)
Dennis J. Williamson	(Reg. No. 32338)
Samuel R. Williamson	(Reg. No. 28768)

I.C. Kizilyalli 9-9-33

Please address all correspondence to the Docket Administrator (Rm. 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P. O. Box 636, Murray Hill, New Jersey 07974-0636. Telephone calls should be made to Scott W. McLellan by dialing 610-712-5118.

Full name of 1st joint inventor: Isik C. Kizilyalli

Inventor's signature Isik C. Kizilyalli Date Dec. 18, 1996

Residence: Orlando, Orange County, Florida

Citizenship: Turkey

Post Office Address: 6535 Doubletrace Lane
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Full name of 2nd joint inventor: Yi Ma

Inventor's signature Yi Ma Date Dec. 18, 1996

Residence: Orlando, Orange County, Florida

Citizenship: China

Post Office Address: 2569 Runyon Circle
Orlando, Florida 32837

Full name of 3rd joint inventor: Pradip Kumar Roy

Inventor's signature Pradip K Roy Date 12/18/1996

Residence: Orlando, Orange County, Florida

Citizenship: United States of America

Post Office Address: 7706 Hidden Ivey Court
Orlando, Florida 32819

08995435-122297



I.C. KIZILYALLI 9-9-33

1/1

FIG. 1

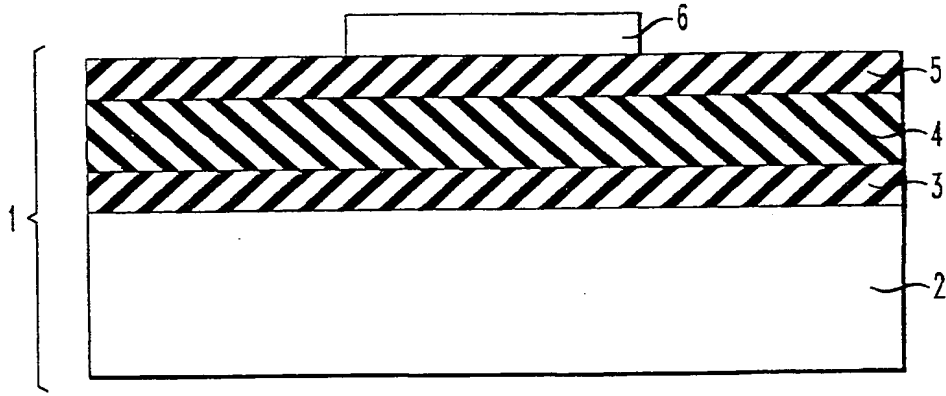
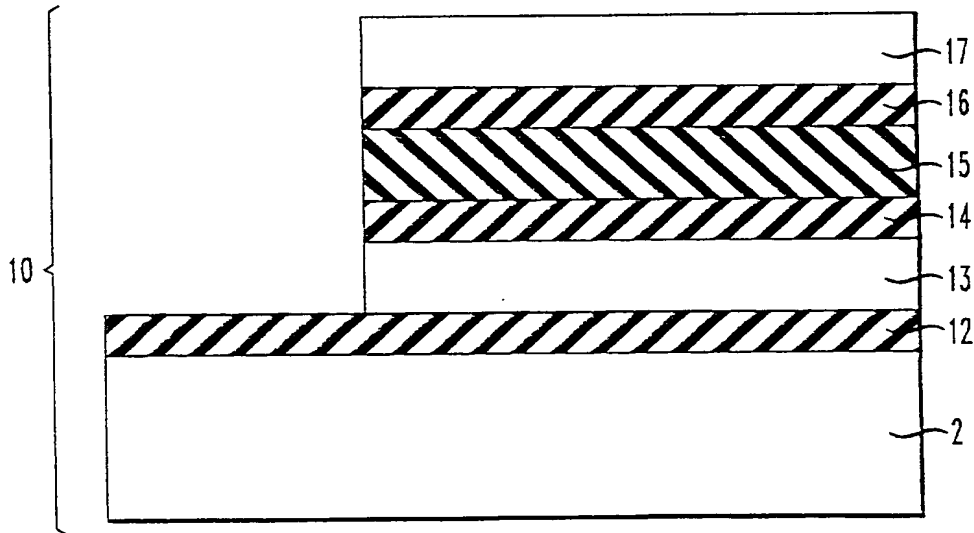


FIG. 2



08095435-12297



IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

#2/A
LEAH
5/14/98

Patent Application

Inventor(s) Isik C. Kizilyalli
Yi Ma
Pradip Kumar Roy
Case 9-9-33
Serial No. 60/033839 Group Art Unit
Filing Date December 23, 1996
Examiner
Title Compound,
High-K,
Gate And Capacitor Insulator Layer

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D. C. 20231

SIR:

PRELIMINARY AMENDMENT

Please enter the following preliminary amendment to the above-identified application:

IN THE SPECIFICATION

Page 1, line 12, change "gets" to --get--;
Page 2, line 22, change "an" to --a--;
Page 3, line 15, change "are" to --is--;
line 27, change "gasses" to --gases--;
line 34, change "improves" to --improve--.

IN THE CLAIMS

Amend claim 8:

- 1 8. The integrated circuit as recited in claim 5, further comprising [step
- 2 of] a conductive layer on the deposited oxide layer.


0895435-122297

Remarks

Please amend the above-referenced application as indicated above.

Respectfully,

Isik C. Kizilyalli
Yi Ma
Pradip Kumar Roy

By 
Scott W. McLellan, Attorney
Reg. No. 30776
610-712-5118

Date: December 22, 1997

0895435-12297